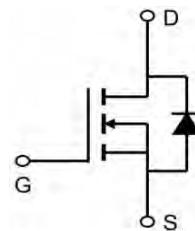


## Description

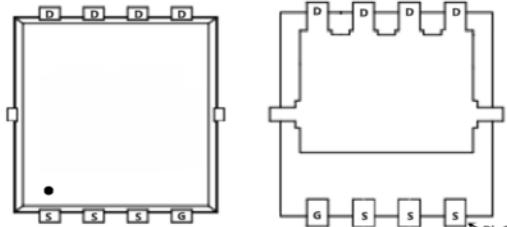
The LM5D120N03 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



## General Features

$V_{DS} = 30V$   $I_D = 120A$

$R_{DS(ON)} < 2.4m\Omega$  @  $V_{GS}=10V$

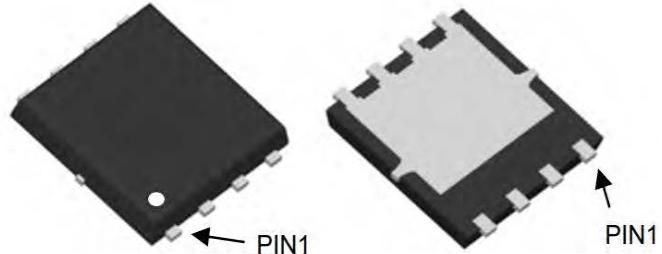


## Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



## Package Marking and Ordering Information

Product ID	Package	Marking	Qty(PCS)
LM5D120N03	DFN5*6-8	AP120N03NF XXX YYYY	5000

## Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	120	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	66	A
$IDM$	Pulsed Drain Current <sup>2</sup>	320	A
$EAS$	Single Pulse Avalanche Energy <sup>3</sup>	180	mJ
$IAS$	Avalanche Current	60	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation <sup>4</sup>	187	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	1.1	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$ , $I_D=250\mu\text{A}$	30	32	---	V
$\Delta BVDSS/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.014	---	$\text{V}/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10\text{V}$ , $I_D=30\text{A}$	---	1.5	2.4	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=15\text{A}$	---	2.5	4.5	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu\text{A}$	1.2	1.5	2.5	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	-4	---	$\text{mV}/^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=24\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$	---	---	1	$\text{uA}$
		$V_{DS}=24\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$ , $V_{DS}=0\text{V}$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=30\text{A}$	---	50	---	S
R <sub>g</sub>	Gate Resistance	$V_{DS}=0\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	---	1.7	---	$\Omega$
Q <sub>g</sub>	Total Gate Charge (4.5V)		---	56.9	---	nC
Qgs	Gate-Source Charge		---	13.8	---	
Qgd	Gate-Drain Charge		---	23.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15\text{V}$ , $V_{GS}=10\text{V}$ , $R_G=3.3\Omega$ , $I_D=1\text{A}$	---	20.1	---	ns
T <sub>r</sub>	Rise Time		---	6.3	---	
Td(off)	Turn-Off Delay Time		---	124.6	---	
T <sub>f</sub>	Fall Time		---	15.8	---	
Ciss	Input Capacitance	$V_{DS}=15\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	---	4345	---	pF
Coss	Output Capacitance		---	340	---	
Crss	Reverse Transfer Capacitance		---	225	---	
IS	Continuous Source Current <sup>1,6</sup>	$V_G=V_D=0\text{V}$ , Force Current	---	---	85	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0\text{V}$ , $I_S=1\text{A}$ , $T_J=25^\circ\text{C}$	---	---	1.2	V

**Note :**

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is  $V_{DD}=25\text{V}$ ,  $V_{GS}=10\text{V}$ ,  $L=0.1\text{mH}$ ,  $I_{AS}=60\text{A}$
- 4、The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.



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LM5D120N03

## Typical Characteristics

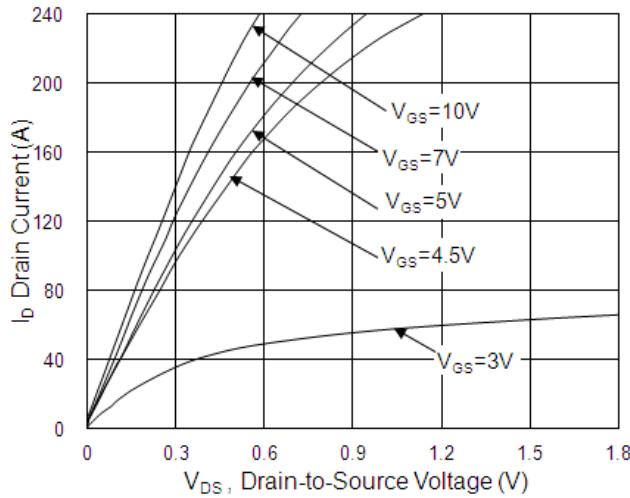


Fig.1 Typical Output Characteristics

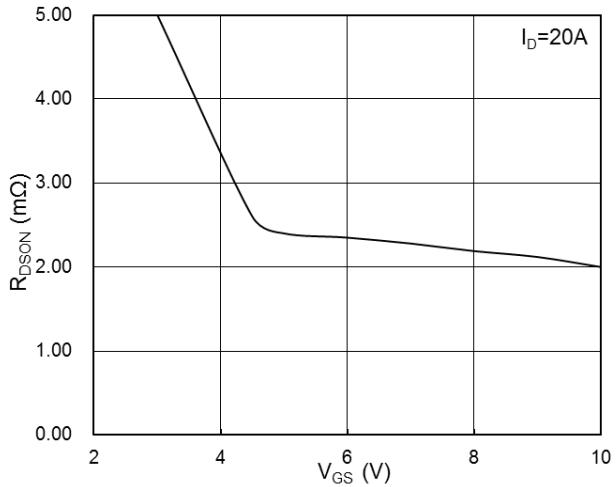


Fig.2 On-Resistance v.s Gate-Source

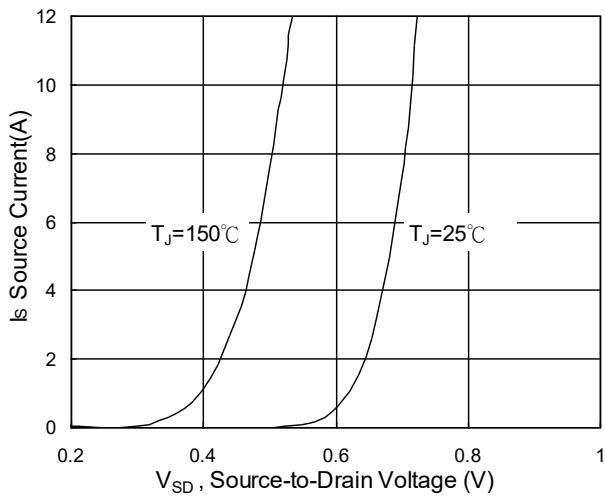


Fig.3 Forward Characteristics of Reverse

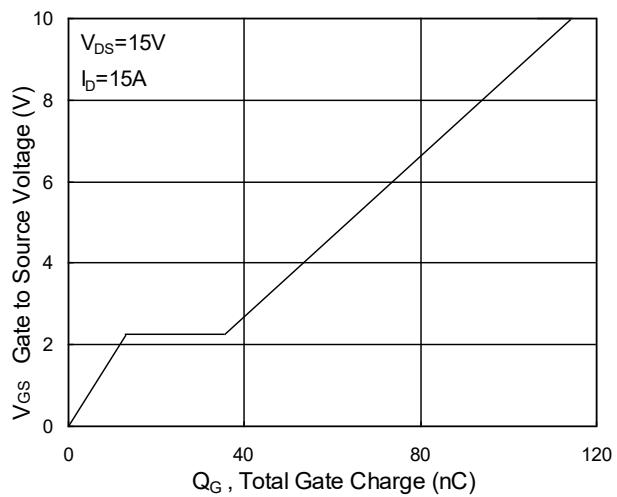


Fig.4 Gate-Charge Characteristics

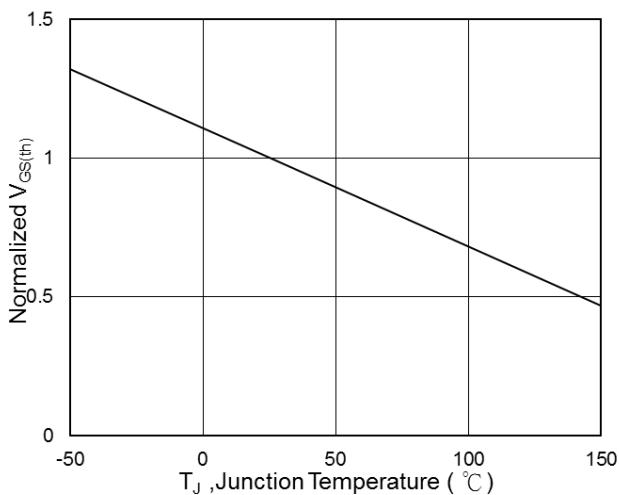


Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$

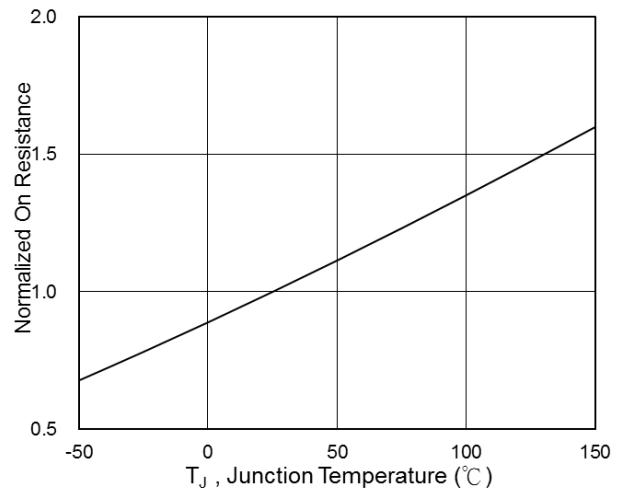
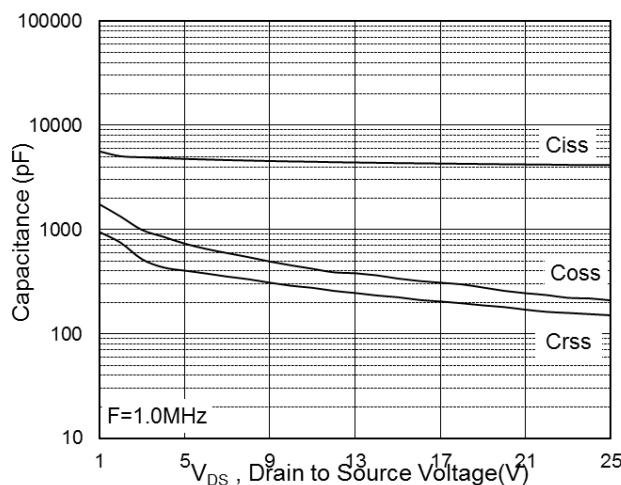


Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$

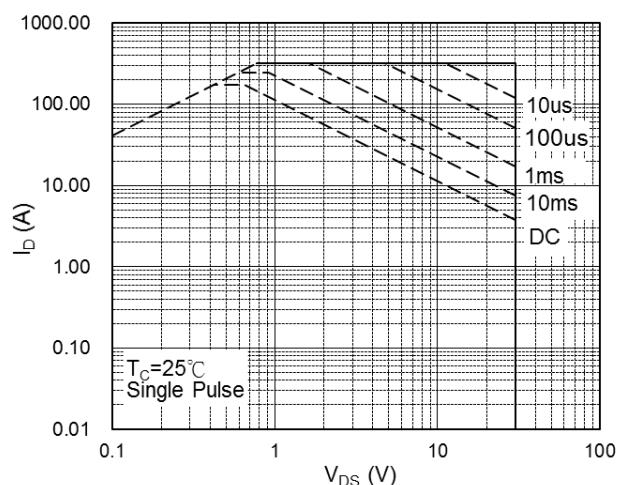


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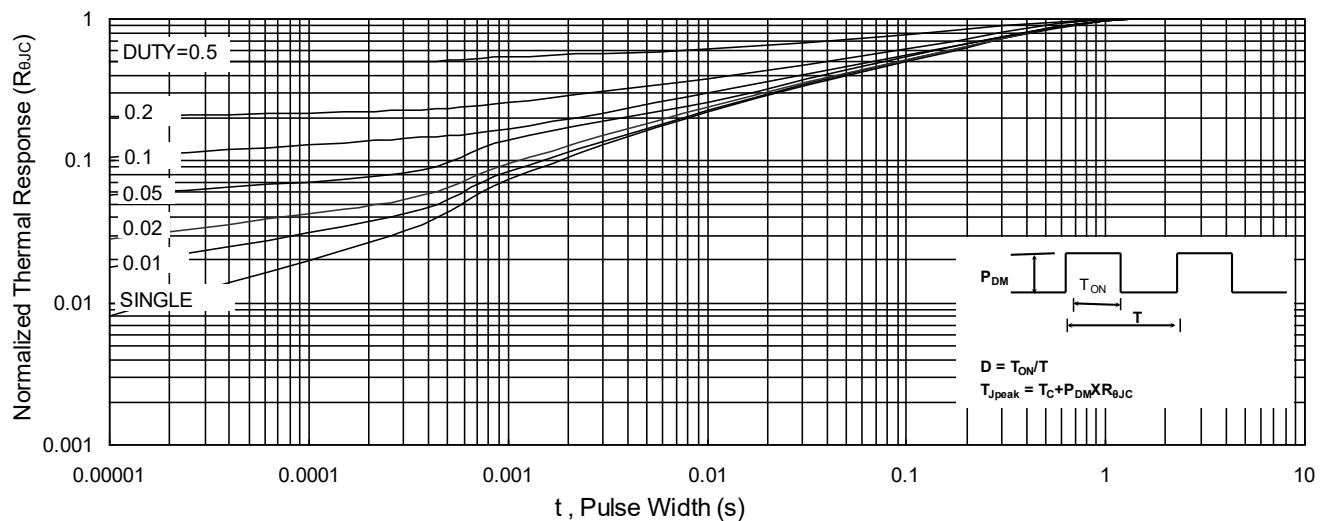
LM5D120N03



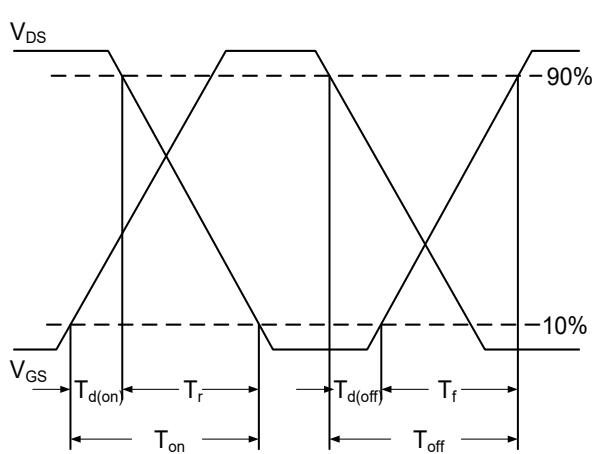
**Fig.7 Capacitance**



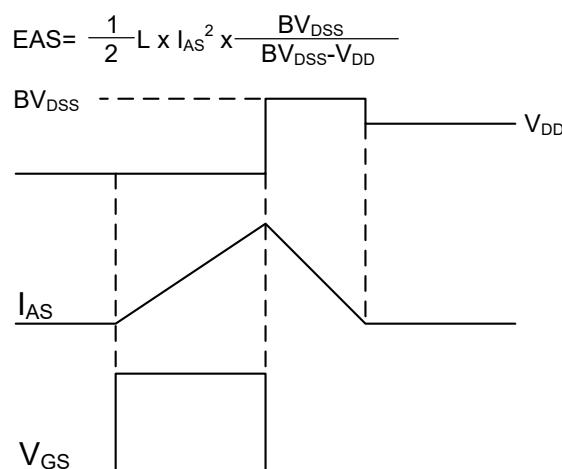
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

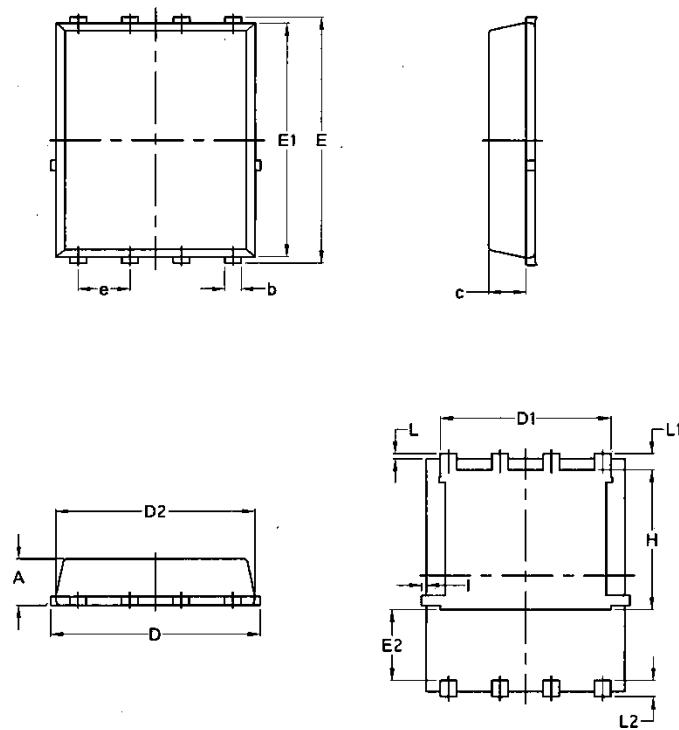


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

## Package Mechanical Data-DFN5\*6-8 Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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