LM8S9P03

-30V P-Channel Enhancement Mode MOSFET

● General Description

The LM8S9P03 combines advanced trench MOSFET technology with a low resistance package to provide extremely low RDS(ON). This device is ideal for load switch and battery protection applications.

● Features

Advance high cell density Trench technology

Low RDS(ON) to minimize conductive loss

Low Gate Charge for fast switching

Dual DIE in one package

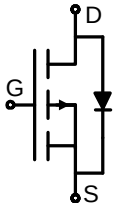
●Application

Power Management in Notebook Computer,

Portable Equipment and Battery

Powered Systems

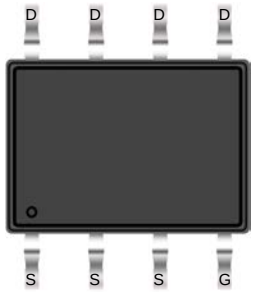
● Product Summary



V_{DS} =-30V I_D =-8A

$R_{DSON(10V\ typ)}$ =13mΩ

$R_{DSON(4.5V\ typ)}$ =17mΩ



SOP-8

●Package Marking and Ordering Information:

Product ID	Pack	Marking	Qty(PCS)
LM8S9P03	SOP-8	TF4435 XXXX YYYY	4000

●Absolute Maximum Ratings (T_C =25℃)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25℃	-8.0	A
	$I_{D@}$TC=75℃	-6.0	A
	$I_{D@}$TC=100℃	-4.8	A
Pulsed Drain Current ①	I_{DM}	-35	A
Total Power Dissipation	P_D@TC=25℃	20	W
Total Power Dissipation	P_D@TA=25℃	0.9	W
Operating Junction Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Single Pulse Avalanche Energy	E_{AS}	30	mJ

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	9.0	° C/W
Thermal resistance, junction - ambient	R_{thJA}	-	-	65	° C/W
Soldering temperature, wavesoldering for 8 s	T_{sold}	-	-	265	° C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V,I_D =-250uA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =-250uA	-1.2	-1.5	-2.5	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-30 V_{GS} =0V	-	-	-1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V ,V_{DS} =0V	-	-	±100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-8A	-	13	18	mΩ
		V_{GS}=-4.5V, I_D=-5A	-	17	25	mΩ
Forward Transconductance	g_{FS}	V_{DS} =-15V, I_D=-8A	-	10	-	S
Source-drain voltage	V_{SD}	Is=-8A	-	-	-1.20	V

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Input capacitance	Ciss	f = 1MHz V_{DS}=-15V V_{GS}=0V	-	1600	-	pF
Output capacitance	Coss		-	350	-	
Reverse transfer capacitance	Crss		-	300	-	

●Gate Charge characteristics(T_a = 25℃)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Qg	V_{DD} = -15V I_D = -8.0A V_{GS} = -10V	-	30.0	-	nC
Gate - Source charge	Qgs		-	5.50	-	
Gate - Drain charge	Qgd		-	8.00	-	

Note: ① Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% ;

Typical Electrical and Thermal Characteristics

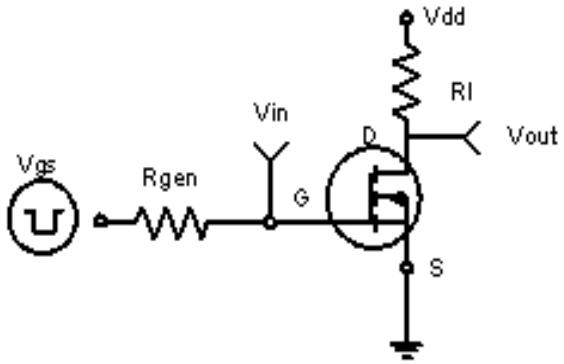


Figure 1:Switching Test Circuit

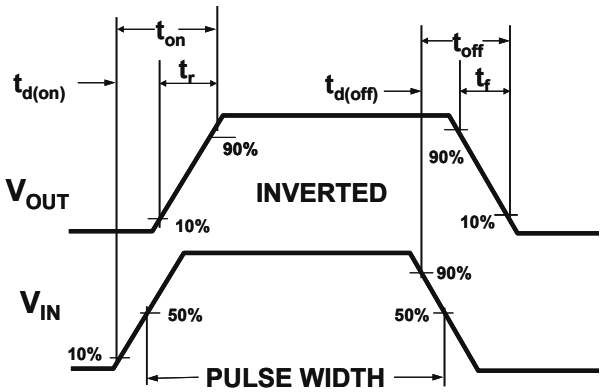


Figure 2:Switching Waveforms

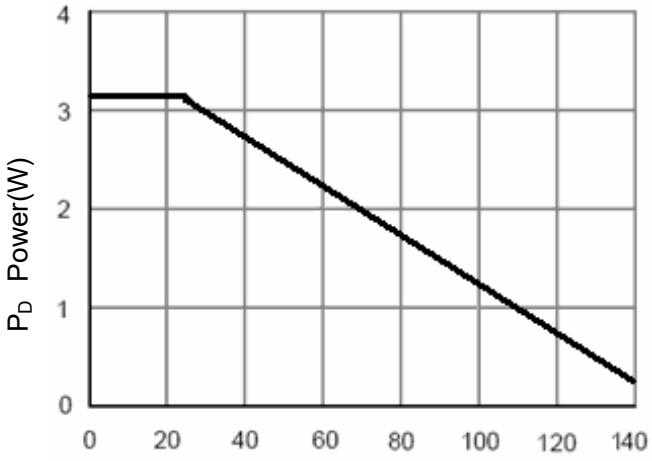


Figure 3 Power Dissipation

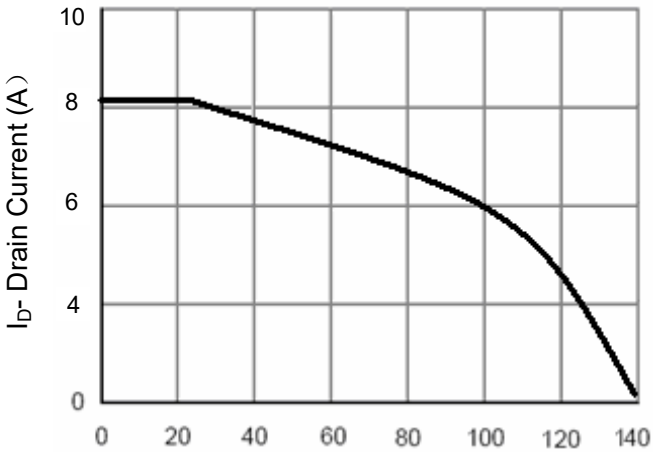


Figure 4 Drain Current

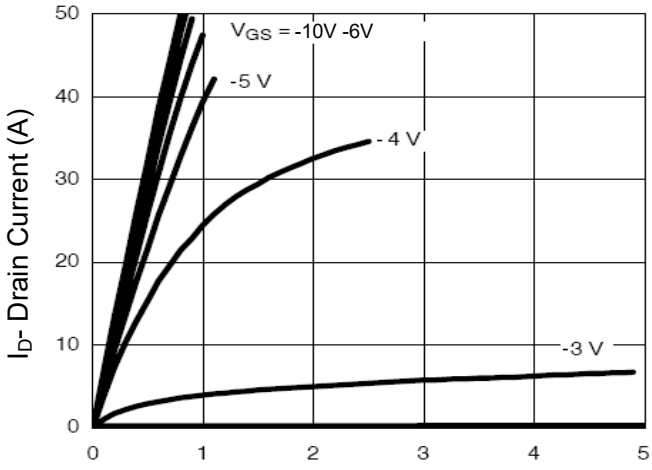


Figure 5 Output Characteristics

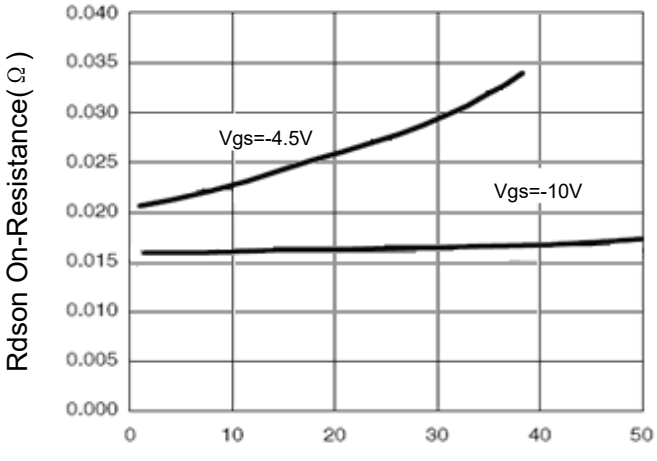


Figure 6 Drain-Source On-Resistance

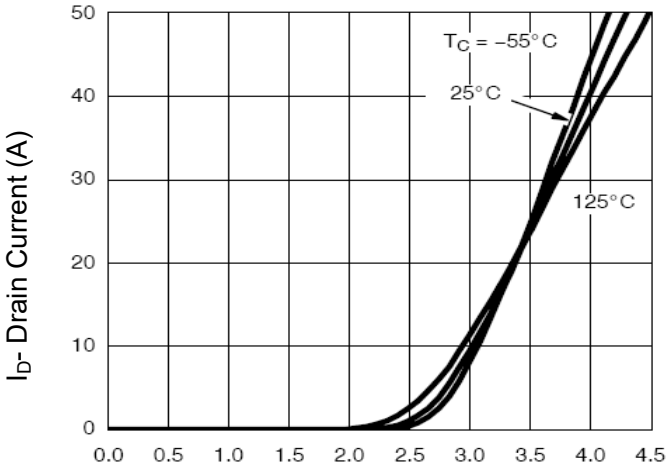


Figure 7 Transfer Characteristics

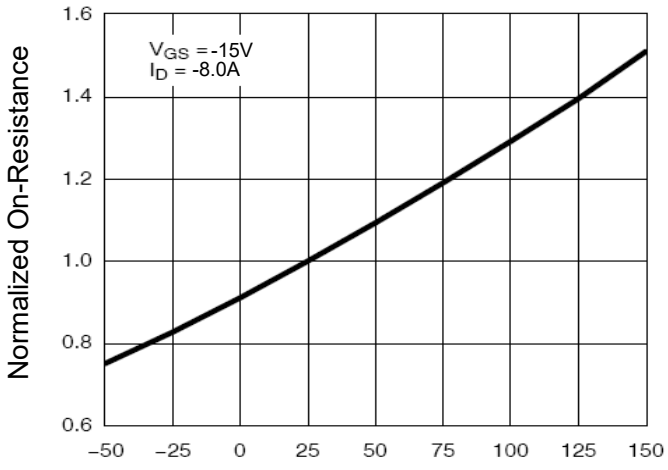


Figure 8 Drain-Source On-Resistance

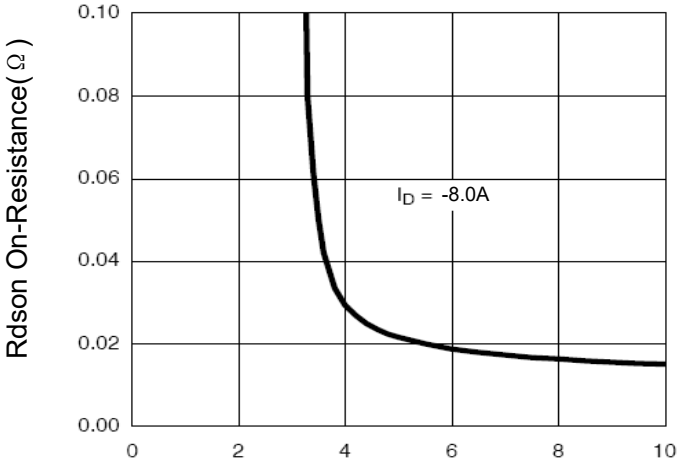


Figure 9 Rdson vs Vgs

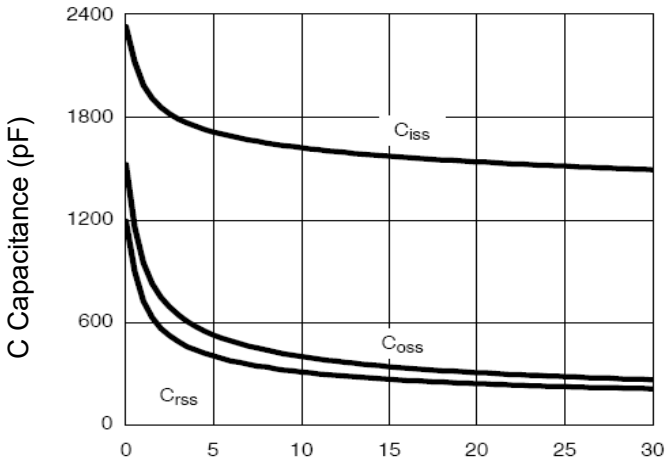


Figure 10 Capacitance vs Vds

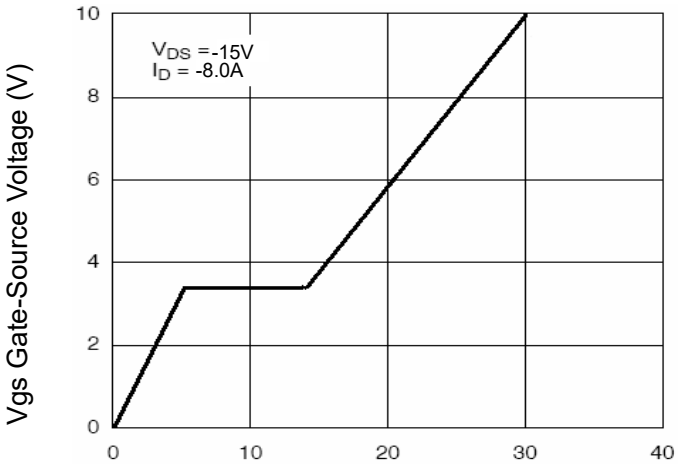


Figure 11 Gate Charge

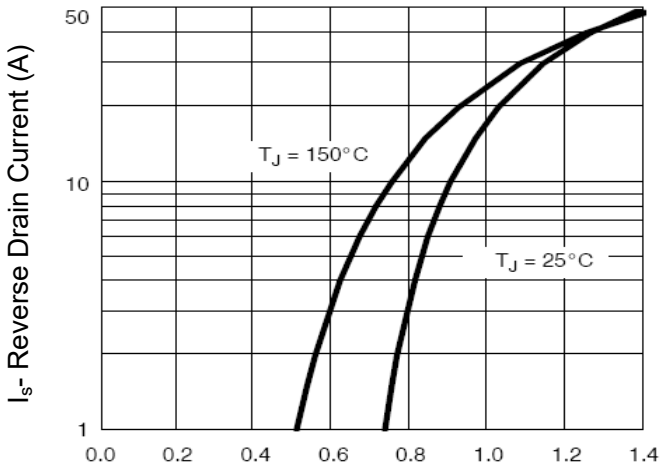


Figure 12 Source- Drain Diode Forward

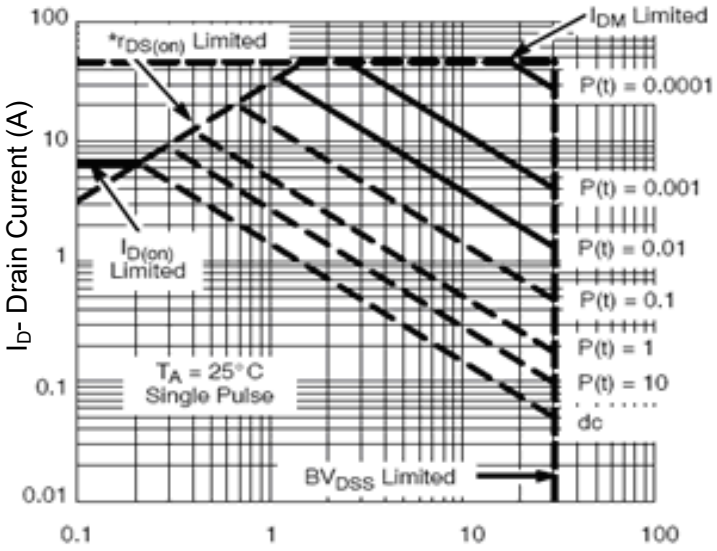


Figure 13 Safe Operation Area

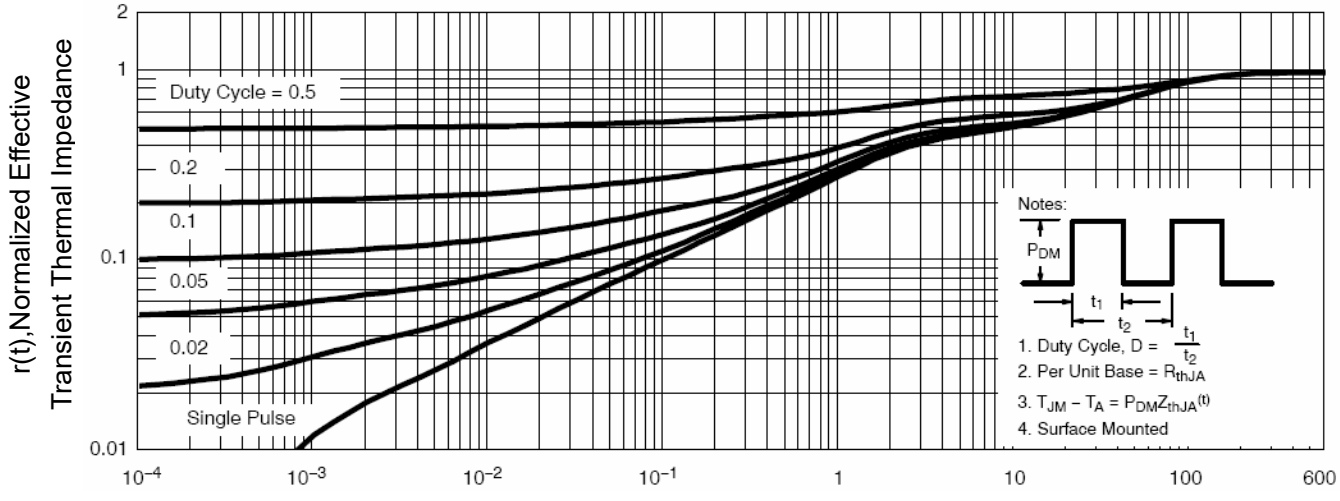
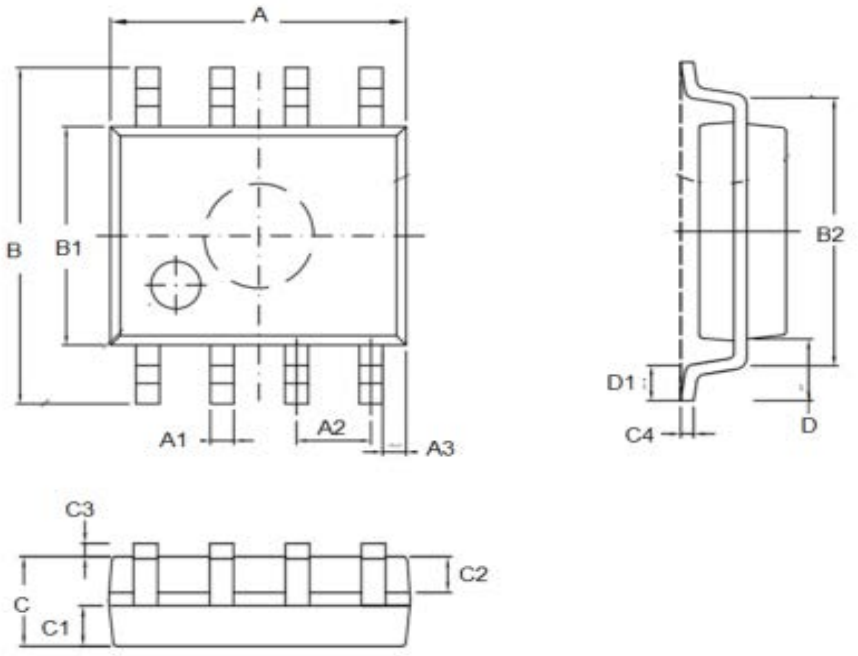


Figure 14 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Outline Dimensions



Unit: mm

SYMBOL	min	TYP	max	SYMBOL	min		max
A	4.80		5.25	C	1.30		1.75
A1	0.37		0.49	C1	0.55		0.75
A2		1.27		C2	0.55		0.65
A3		0.41		C3	0.05		0.20
B	5.80		6.20	C4	0.10	0.20	0.23
B1	3.80		4.10	D		1.05	
B2		5.00		D1	0.40		0.62

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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